CLAIMS

1. (Previously Presented) A circuit for generating a plurality of phases of an input signal comprising:

a phase generator operable as a voltage controlled oscillator and as a voltage controlled delay line, said phase generator comprising a plurality of delay blocks;

a phase detector coupled in a first feedback loop with said phase generator, said phase detector for comparing said input signal with a first output signal of said phase generator when in an delay lock mode and for generating a first control signal to said phase generator to switch from said delay lock loop mode to said phase locked loop mode; and

a phase-frequency detector coupled in a second feedback loop with said phase generator said phase frequency detector for comparing said input signal with a second output signal of said phase generator when in a phase locked loop mode.

2. (Original) The circuit of Claim 1 further comprising a delay element disposed in said second feedback loop between said phase generator and said phase-frequency detector and wherein said delay element generates an output signal.

3. (Cancelled).

4. (Previously Presented) The circuit of Claim 2 wherein said phase generator is operable for generating a plurality of phases of a second output signal when operating in said phase locked loop mode.

5. (Original) The circuit of Claim 1 wherein each of said plurality of delay blocks comprises a plurality of delay elements coupled in series.

6. (Original) The circuit of Claim 5 wherein each delay block is associated with a respective multiplexer for configuring a number of said plurality of delay elements coupled in series.

7. (Previously Presented) The circuit of Claim 6 wherein a second control signal generated by said phase detector causes said multiplexers to dynamically select the number of said plurality of delay elements that are coupled in series.

8. (Previously Presented) The circuit of Claim 5 wherein a second control signal generated by said phase-frequency detector controls a delay time of each of said plurality of delay elements.

9. (Original) The circuit of Claim 8 wherein said circuit suppresses skew of said plurality of phases of said input signal.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Canceled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)